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Report on “A learnable parallel processing architecture towards unity of memory and computing”

Virtually all modern machines utilize von Neumann architecture, the stored memory and program concept from nearly 80 years ago. As technology progresses, this architecture is constrained by the physical separation of memory and processing units resulting in a higher energy cost due to power dissipation. The authors present a novel, energy-efficient architecture, “iMemComp,” based on resistive switching (RS) devices that combine memory and processing into a single unit.

The authors report that iMemComp are able to perform the same operations, such as AND, OR, INVERT, NAND, and XOR, as existing machines utilizing von Neumann architecture but at a fraction of the cost in terms of power dissipation because of the “learning” ability of the RS that reduces power consumption based on repetitive circuit use. Additionally, the parallel nature of RS adders allows a 76.8% increase in speed when compared to existing complementary metal-oxide-semiconductor (CMOS)adder circuits. Finally, the physical circuit area of the RS-based 32-bit adder is 700 times smaller than comparable CMOS adder circuits.

Upon reading this paper in-depth, I realize that this study is more in the realm of electrical engineering than it is in computer architecture, however, the thought of moving away from von Neumann architecture towards RS architecture that, at first glance, seems much more efficient, would have far-reaching implications in terms of computer architecture in the future.

**References**

[1] H. Li, B. Gao, Z. Chen, Y. Zhao, P. Huang, H. Ye, L. Liu, X. Liu & J. Kang. “A learnable parallel processing architecture towards unity of memory and computing,” *Scientific Reports (Nature Publisher Group),* vol. 5, no. 13330, August, 2015. [Online serial]. Available : <https://www.nature.com/articles/srep13330> [Accessed February 2, 2019].